

HyperLynx EXT includes a complete suite of tools for pre- and post-layout signal integrity, crosstalk and EMC analysis.

Major product benefits:

- Identify and resolve SI problems before costly layout, prototyping, test cycles and volume production
- Industry-leading ease-of-use
- Pre-and post-layout analysis is compatible with all major PCB layout and routing applications
- Differential signal simulation and analysis, including differential impedance, and optimization of differential terminations
- Terminator Wizard™ recommends optimal termination strategies, including series termination, parallel, parallel AC and differential
- Provides an early look at likely EMC failures, including both radiation and trace current analysis

Overview

Increasingly fast edge-rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing volume of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail-making otherwise excellent designs stare blankly into space.

HyperLynx® EXT, including LineSim™ for pre-layout analysis and BoardSim™ for post-route analysis, targets designs at frequencies up to about 300 MHz. At higher speeds, transmission-line losses (including skin effect and dielectric loss) and via parasitics take on gradually increasing importance; the HyperLynx GHz bundle models all of these effects and includes features that address the special needs of gigabit-per-second, SERDES designs.

Complete SI and EMC Analysis Suite

Signal integrity and timing analysis, for most engineers, is only one of many systems design tasks. A software tool that's easy to learn and easy to relearn is a necessity with today's schedule pressures.

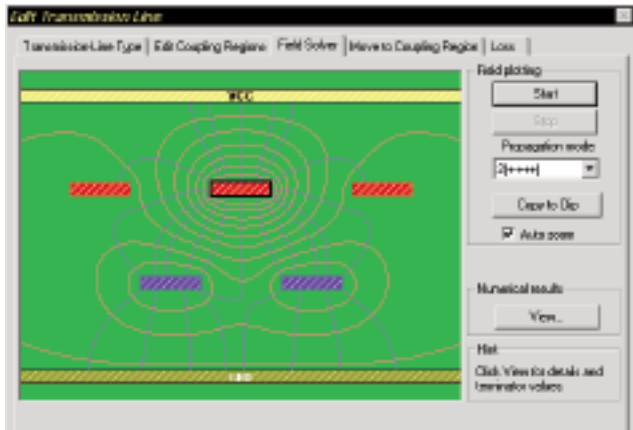
Hardware engineers, PCB designers and signal integrity specialists alike can use HyperLynx as a team; getting simulation results without requiring weeks of software training. The emphasis is on getting designs right the first time, avoiding costly overdesign, and saving recurrent layout, prototype and test cycles in the lab.

With HyperLynx, you can address high-speed PCB problems throughout the design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The process is as easy as using an oscilloscope or spectrum analyzer in the lab, and at a fraction of the cost.

LineSim EXT

Pre-layout simulation with LineSim, part of HyperLynx EXT, allows you to predict and eliminate signal integrity problems early to proactively constrain routing, plan stackups, and optimize clock, critical signal topologies, and terminations prior to board layout. LineSim's intuitive point-and-click transmission-line modeling approach is an ideal way to "get it right" the first time.

- Quickly enter complex interconnect scenarios, including ICs, transmission lines, cables, connectors and passive components
- Simulate immediately, using industry-standard IBIS models, HyperLynx's 18,000 model IC library, generic models, or build custom models from databook information
- Experiment with stackup options where impedance recalculation is automatic
- Visual IBIS Editor allows you to check and edit IBIS models including a hierarchical, newer, automated syntax checking V/I-V/t auto-correction and drag and-drop curve editing
- Antenna Current Probe provides invaluable insight into the root cause of most EMC problems, such as excessive energy in critical nets on the PCB



Pre-layout crosstalk analysis allows you to optimize spacing, stackup and termination.

To learn more about high-speed design and HyperLynx software, visit www.mentor.com/hyperlynx to download the high-speed design tutorial, or call to schedule a product demonstration.

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BoardSim EXT

Post-layout signal integrity simulation with BoardSim, part of HyperLynx EXT, allows you to analyze signal integrity and timing at three important stages: following part placement in your PCB layout system, after critical net routing and after detailed routing of an entire board.

- Batch simulation scans high-speed nets in batch mode, checking against min. and max. delay values, crosstalk and over/undershoot limits for each net; automatically producing intuitive reports, including a spreadsheet-compatible list of signal integrity, crosstalk and EMC hot spots on your board
- Interactive analysis takes you to the next level, analyzing batch simulation trouble spots
- Quick Terminators allow new termination components to be inserted on the fly
- Spectrum Analyzer shows predicted radiation at every frequency, compared to FCC, CISPR, and VCCI limits. Analysis takes a fraction of the time, compared to finding emission sources downstream in an anechoic chamber

BoardSim-compatible PCB layout systems:

- Mentor Graphics PADS® Layout, Expedition™ and Board Station®
- Cadence Allegro, SPECCTRA and OrCAD Layout
- Altium Protel and P-CAD
- Zuken CADStar, Visula, CR3000/5000 PWS and BD

Minimum Hardware/Software Requirements

Windows XP or 2000

- Pentium II 333 MHz CPU, or faster
- 128 MB RAM; 60 MB hard disk space
- 1024 x 768, 256 color display
- NIC, Parallel port, or USB port to supply HostID to license management software
- 165 MB for Extended IBIS Libraries

Sun Solaris version 8 or 9:

- 320 MB hard disk space
- 165 MB for Extended IBIS Libraries
- Recommended Patch Cluster: March 19, 2002 or later
- Mach 64 Graphics card patch: 108606-31 or later

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